Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A method of accessing data from a low pin count (LPC) memory and a firmware memory comprising:

receiving an input signal comprising a 1-bit memory flag; and

accessing data from the LPC memory or the firmware memory according to the memory flag.

Claim 2 (Original): The method of accessing data from an LPC memory and a firmware memory in claim 1 wherein the input signal further comprises an accessing address and an accessing flag.

Claim 3 (Original): The method of accessing data from an LPC memory and a firmware memory in claim 2 wherein accessing data from the LPC memory or the firmware memory is according to the accessing address.

Claim 4 (Original): The method of accessing data from an LPC memory and a firmware memory in claim 2 wherein accessing data from the LPC memory or the firmware memory is according to the accessing flag.

Claim 5 (Original): The method of accessing data from an LPC memory and a firmware memory in claim 1 further comprising resetting all previous instructions.

Claim 6 (Currently Amended): A computer system comprising:

an interface circuit for receiving an input signal comprising a 1-bit memory flag,

the interface circuit comprising a flag reading unit for reading the memory flag of the input signal, the interface circuit for accessing data from an LPC memory or a firmware memory according to the memory flag; and

an address storage unit for storing an accessing address of the LPC memory or the firmware memory.

Claim 7 (Original): The computer system in claim 6 wherein the input signal further comprises the accessing address and an accessing flag, which defines whether data is to be read from or written into the LPC memory or the firmware memory.

Claim 8 (Currently Amended): The computer system in claim ~~6 further comprising an LPC memory and a firmware memory~~ 7 wherein the address storage unit receives and latches the accessing address from the input signal.

Claim 9 (New): A method of accessing a first or second memory, the method comprising:

selecting the first memory or the second memory for data access according to a 1-bit memory flag comprised by an input signal;

latching a memory address be accessed, the address comprised by the input signal;

confirming a latched address is within the selected memory;

receiving an accessing flag comprised by the input signal to determine whether to read data from or write data to the latched address; and

reading data from or writing data to the latched address according to the accessing flag.

Claim 10 (New): The method of claim 9 wherein the first memory is a low pin count (LPC) memory and the second memory is a firmware memory.

Claim 11 (New): A device comprising an address storage unit for latching the address, an interface unit connecting the address storage unit, the first memory, and the second memory, the interface unit comprising a flag reading unit for determining whether the selected memory is to be written to or read from, the device utilizing the method of claim 10.